Universal Logic Gate: ENOR

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Abstract. ***This paper discusses about additional (derived) universal logic gate useful in the binary circuit, namely ENOR (Emergency NOR) on the base of NOT gate; The proposed logic gates are differ from the existing universal gates; to handle the must/emergency conditions, such as after starting any process the condition is to stop a process at any scenario until the process get completed. The proposed gate was well defined and simulated with well-defined truth table. The simulation result shows that the working principle of ENOR was well defined with truth tables, algebraic formula and efficiency.***

Keywords: ENOR, NOR gate, OR gate, emergency gate, NOT gate;

I. Introduction

In electronics, logic gates are the fundamental building blocks of all digital systems. All the existing basic logic gates or derived logic gates were designed to produce a logical/binary out; in some cases to convert all values to produce the desired binary out is not possible by a single gate; for example to convert all binary values to ZERO or ONE. The proposed ENOR logic gate can be used based on the requirements to get the desired binary out [1-20].

II. NOT gate

NOT gate has one-input and one-output. It is a logic circuit whose output is always the complement of the input. Fig.1 indicates the logic symbol and truth table of NOT gate along with simple implementation using switches.

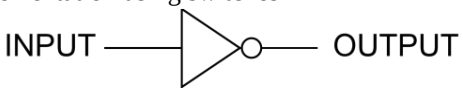

Fig.1: NOT gate graphic symbol

The purpose of inverter is to change one logic level to opposite level. The LOW level at input produces a HIGH level and vice versa. In terms of bits, it changes a 0 to a 1 and a 1 to 0.

III. ENOR Logic Gate

In digital logic, a ENOR or ENOR gate is a logic gate which converts its input to 1 (ONE) or HIGH. The main purpose of a ENOR is to convert any input to HIGH. ENOR has one input and one output; its output always HIGH; simply, ENOR is a very basic active device that generates 1 as output; ENOR gate symbolically shown in Fig. 2.

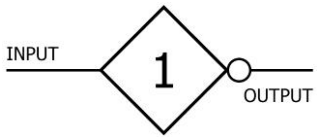

Fig.2: Proposed ENOR gate graphic symbol

A. Truth Table

The Truth Table shows the values of the circuit output for all input values or the Truth Table shows a logic circuit's output response to all of the input combinations.

INPUT (A)	OUTPUT (F) $F = \bar{A} + A$
0	1
1	1

Table.1: ENOR gate Truth Table

i. Algebraic Function

The process of converting control objectives into a ladder logic program requires structured thought. Boolean algebra provides the formula needed to analyze and design these systems. The algebraic formula of the proposed ENOR gate is below. Logic gates are electronic circuits that implement the basic functions of Boolean Algebra.

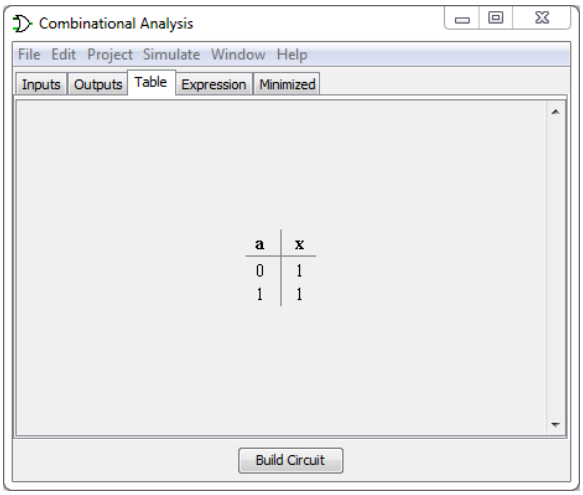

Fig.3: ENOR gate Truth Table (LOGISIM, Ver: 2.7.1)

Boolean Algebra is the mathematical foundation of digital circuits. Boolean Algebra specifies the relationship between Boolean variables which is used to design combinational logic circuits using Logic Gates.

$$F = \bar{A} + A \qquad \text{---------- (1)}$$

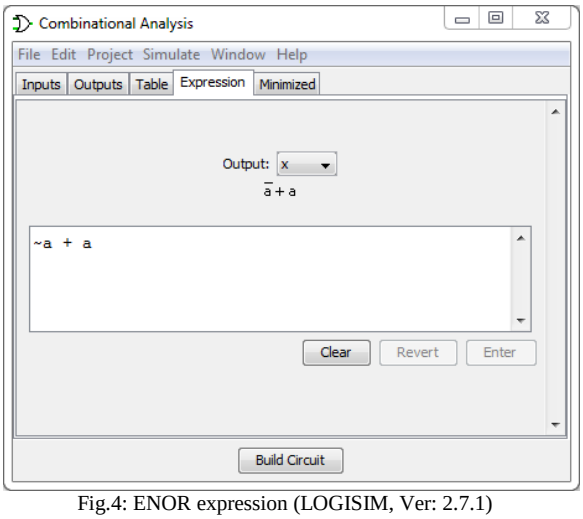

Fig.4: ENOR expression (LOGISIM, Ver: 2.7.1)

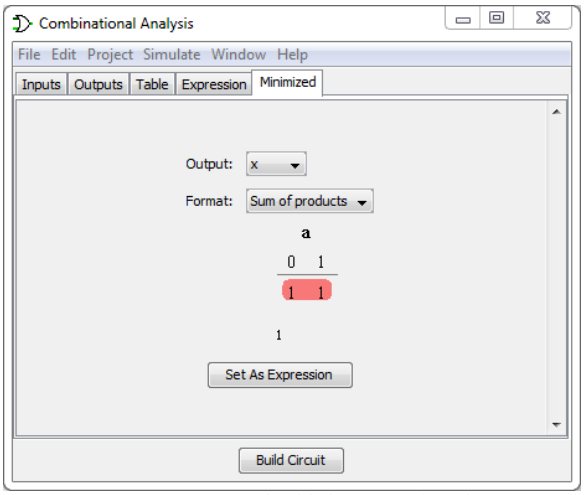

Fig.5: ENOR gate Truth table by 'Sum of Product'

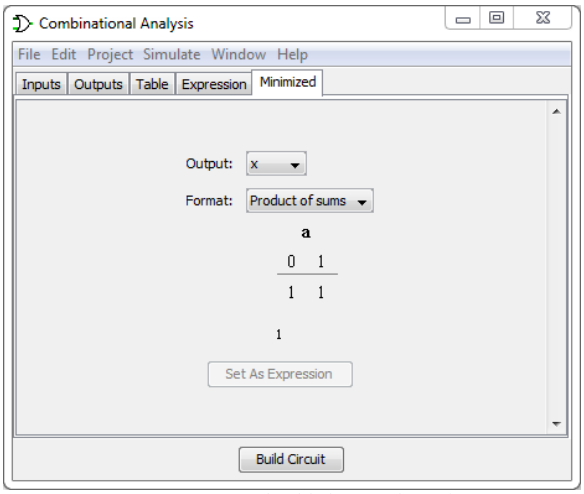

Fig.6: ENOR gate Truth table by 'Product of Sum'

ii. Detailed Graphic Symbol

The ENOR is a combination of both NOT and OR gates; so that the output of NOT gate is fed as one input of the OR gate and for another input it shares the NOT gate input to produces the output. Fig.3 shows the detailed working principle.

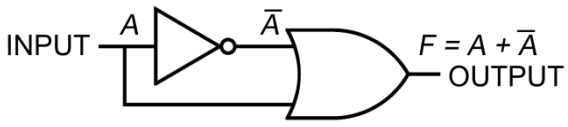

Fig.7: ENOR gate detailed graphic symbol

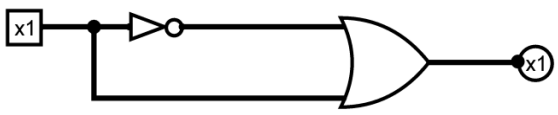

Fig.8: ENOR gate structural output of LOGISIM

III. Result & Discussion

The well-defined truth table, algebraic formula and detailed working principle shows the gate perfectness. The gates where simulated under LOGISIM 2.7.1(version) on different modes with following specifications.

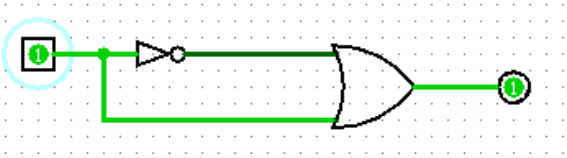

Fig.9: ENOR gate Ladder Mode Output – Input ON

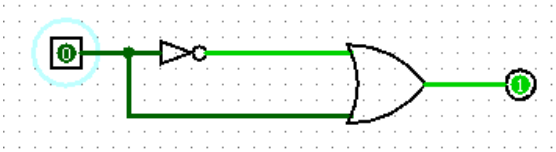

Fig.10: ENOR gate Ladder Mode Output – Input OFF

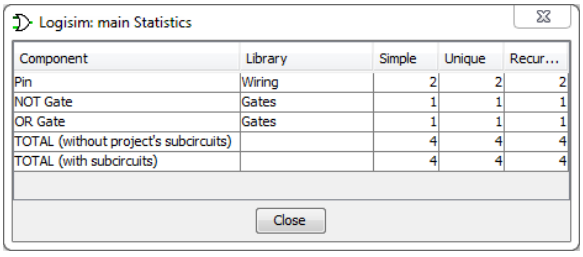

Fig.11: ENOR gate Statistics

Device Report

- LOGISIM V 2.7.1
- SA2 – Type of the PLC
- Tick Frequency – 1Hz
- Ladder Diagram- High level language

V. Conclusion

The proposed ENOR gate was simulated and tested; the clock output, the well-defined algebraic equation and Truth table shows the clear working principal of the gate. This gate can be used for various purposes such as to minimize the complicated circuits, as a switch etc... In the digital electronic as an addition to improve the technology.

The ENOR gate is a basic digital logic gate that implements logical conjunction - it behaves according to the truth table to the right. A HIGH output (1) results for all the inputs to the ENOR gate. If none or not all inputs to the ENOR gate are HIGH or LOW, a HIGH output results.

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